REMARKS

Claim 1 is amended to correct a typographical error.

New claims 22-31 are added to claim the invention in alternative language. The new claims are supported by the specification, and no new matter has been added.

The Office Action does not establish that claims 1-21 are unpatentable under 35 USC §103(a) over US patent number 6,044,211 to Jain (hereinafter, "Jain"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by Jain, fails to provide a proper motivation for modifying the teachings of Jain, and fails to show that the modification could be made with a reasonable likelihood of success.

As to the limitations of claim 1, for example, the Office Action does not show that Jain teaches the limitations of the claimed method for re-targeting a design. The claimed method includes receiving a first low-level design representation targeting a first integrated circuit; transforming said first low-level design representation into a synthesizable, editable, and simulatable high-level design representation; and processing said high-level design representation to generate a second low-level design representation targeting a second integrated circuit.

The Office Action does not establish that Jain suggests the limitations of receiving the first low-level design representation targeting a first integrated circuit. Jain's FIGs. 4 and 5 are cited. But Jain's element 164 appears to show that a low-level design is the final output, not being received for processing. The Office Action also cites Jain's col. 9, l. 48 - col. 12. However, Jains' col. 11 illustrates an RTL listing, which the present application characterizes as a high-level design description, not a low-level design description (spec. para. #3). In Jain's col. 16, ll. 28-60, which was cited by the Office Action, Jain describes nodes and subnodes in a graph hierarchy. There is no apparent indication of receiving a

low-level design representation. Furthermore, none of the cited sections suggest that a design representation is targeted to any particular integrated circuit. Therefore, the Office Action does not establish that Jain receives a low-level design representation.

The Office Action does not establish that Jain suggests the limitations of transforming the low-level design representation into a synthesizable, editable, and simulatable high-level design representation. The Office Action cites Jain's col. 19, l. 44 - col. 22. However, this section describes a simulation model. There is no specific teaching of Jain cited to indicate that Jain's simulation model is transformed from a low-level design representation. Other portions of Jain appear to teach the opposite of that claimed: Jain's simulation model is prepared from a high-level design. Therefore, the Office Action does not establish that Jain transforms the low-level design representation into a synthesizable, editable, and simulatable high-level design representation.

As to the limitations of processing the high-level design representation into a low-level design representation for a second IC, the Office Action does not establish that Jain suggests these limitations. The cited sections of Jain discuss mapping of data path hardware instances and functions to representative graph nodes. There is no apparent suggestion of any targeting of a second IC.

The claim clearly requires a first and a second IC, and Jain's tool initiates the modeling using a top-down approach beginning with a behavioral level and automatically synthesizing and verifying to a lower level structural description that fully encompasses not only the data path structure but also the Boolean expressions of timed control signals which operate upon the structure (col. 4, ll. 48-55). There is no apparent mention of a low-level design targeted to a second IC being generated from a low-level design targeted to a first IC. Further

explanation is respectfully requested if the rejection is maintained.

The Office Action also does not provide any evidence of a motivation to modify the teachings of Jain. Nor is it apparent how Jain could be successfully modified to achieve the claimed invention. The rejection of claims 1-21 over Jain should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

Claims 2-5 depend from claim 1 and are patentable over Jain for at least the reasons set forth above.

As to claims 6-9, claims 6-8 indicate specific high-level design representations, and claim 9 indicates a specific low-level design representation. The Office Action does not cite any teaching of Jain that suggests transforming any particular low-level design representation into any one of these specific high-level representations. Therefore, *prima facie* obviousness is not established for claims 6-9.

Claim 10 includes further limitations of the transforming the low-level design into the high-level design representation including parsing the first low-level design representation; identifying equations in said first low-level design representation that give rise to synthesizable and simulatable objects; and writing said high-level design representation that contains said synthesizable and simulatable objects. The teachings of Jain alleged to suggest these limitations appear to describe a simulation model prepared from a high-level design. There is no apparent suggestion of preparing a simluation model from a low-level design as claimed. Therefore, *prima facie* obviousness is not established for claim 10.

Claims 11-21 depend from claim 10 and are allowable over Jain for at least the reasons set forth above.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the amendments and remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patent, P.O. Box 1450, Alexandria, VA 22313-1450, on July 21, 2004.

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